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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/931,131	08/16/2001	Hyungwon Kim	UOM 0209 PUSP	3611

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EXAMINER	
WHITMORE, STACY	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 10/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/931,131	KIM ET AL.	
	Examiner	Art Unit	
	Stacy A Whitmore	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *7/22/03* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) *39-45* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-45* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

FINAL ACTION

1. Newly submitted claims 39-45 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: Newly presented claims are related as a species of claims 1-38.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 39-45 withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3, and 6-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Pal, Ajit, et al., "Synthesis of Two-level dynamic CMOS circuits".

3. As for claims 1-3, and 6-7, Pal disclosed the invention as claimed, including a method for synthesizing a circuit representation having an initial unateness into a new circuit representation having greater unateness wherein the circuit has a function [pg. 82, , section 1, paragraph 2;], the method comprising:

(i) partitioning the circuit representation to obtain a representation of at least one sub-circuit [pg. 84, section 3, the function f is decomposed into a sum of factors

(examiner interprets as equivalent to sub-circuits) which are partitioned from an initial Boolean function];

(ii) recursively decomposing the representation of the at least one sub circuit [pg. 83, section 2, second paragraph, lines 4-8, where the minterm is explained and used herein for reference to the MUD; pg. 86 section 4, lines 1-4 (MUD); pg. 87, sections 5 and 5.1 "transform IUD to a MUD, section 5.2, step 2, (examiner interprets the algorithm hear to decompose the circuit representation into a circuit representation with greater unateness because there are less terms in the circuit after the decomposition, which reads on a greater unateness]; and

(iii) merging the representation sum-of-products (SOP) or product-of-sums (POS) representation into the circuit representation to form a new circuit representation having a unateness greater than the initial unateness while maintaining the function of the circuit substantially unchanged [see as cited in (ii), the circuit is transformed in to a (MUD) which is a merging of the terms].

[claim 2] repeating steps [(i), (ii), and (iii) until a desired level of unateness for the new circuit representation has been achieved] [pg. 87, section 5.1, steps 1-3.].

[claim 3] wherein the SOP or POS representation selected for each decomposition is the representation having fewer binate variables [5.1 "transform IUD to a MUD, section 5.2, step 2, (examiner interprets the algorithm hear to decompose the circuit representation into a circuit representation with greater unateness because there are less terms in the circuit after the decomposition, which reads on a greater unateness, which also reads as fewer binate variables].

[claim 6] wherein the circuit is a digital circuit [abstract].

[claim 7] wherein the representation of the at least one sub-circuit is highly unate [pg. 84, section 3 shows the initial unate function].

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-7 are rejected under 35 U.S.C. 102(e) as being anticipated by Chakrabarti, et al., "Synthesis of symmetric functions for path-delay fault testability".

5. As for claims 1-7, Chakrabarti disclosed the invention as claimed, including a method for synthesizing a circuit representation having an initial unateness into a new circuit representation having greater unateness wherein the circuit has a function [pg. 1077, left hand side, synthesis technique, fig. 1], the method comprising:

(i) partitioning the circuit representation to obtain a representation of at least one sub-circuit [pg. 1077, fig. 1; section A., sub-circuit function is decomposed into unate functions and then resulting in a composite circuit; pg. 1078 section IV also shows a union of several functions derived from unate decomposition, examiner interprets the cited sections to have a higher unateness because the number of terms in the final circuit representation are less than the original, which is a higher unateness];

(ii) recursively decomposing the representation of the at least one sub circuit [see as cited in step (i), the unate decomposition is a recursive step.]; and

(iii) merging the representation sum-of-products (SOP) or product-of-sums (POS) representation into the circuit representation to form a new circuit representation having

a unateness greater than the initial unateness while maintaining the function of the circuit substantially unchanged [see as cited in section (i), the union of functions, figs. 1 and 2 show the final circuit representation which is a merging of sub-circuits; see also pg. 1079, section B. algorithm shows the merging (union of SOP terms into P)].

[claim 2] repeating steps [(i), (ii), and (iii) until a desired level of unateness for the new circuit representation has been achieved] [pg. 1079, section B., see repeat .... until].

[claim 3] wherein the SOP or POS representation selected for each decomposition is the representation having fewer binate variables [on pgs. 1077-1079, the selected sub-circuit representations have fewer binate variables because they are selected as unate to begin with.].

[claim 4] merging common expressions of the SOP or POS representations [pg. 1079, union of group 1 and group 2].

[claim 5] wherein algebraic division is used to merge common unate expressions of the SOP or POS representation [pg. 1079, section B. output – is a algebraic division].

[claim 6] wherein the circuit is a digital circuit [pg. 1077, figs. 1 and 2 show a digital circuit representation].

[claim 7] wherein the representation of the at least one sub-circuit is highly unate [pg. 1077, left hand side, the unate sub-circuits 1 and 2].

6. Claims 10-17, 19, 20-28, 29-35, and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chakrabarti, et al., "Synthesis of symmetric functions for path-delay fault testability" in view of Rostoker (US Patent 6,470,482).

7. As for claims 10-17, 19, 20-28, 29-35, and 38, Chakrabarti disclosed the invention substantially as claimed, including the method of synthesizing a circuit representation including receiving input and output as cited above in the rejections of claims 1-7 (Chakrabarti).

Charkrabarti did not specifically disclose the method performed on a system (means for – e.g. computer system with computer readable medium having instructions for executing the program), and input and output in HDL.

Rostoker disclosed, a method performed on a system (means for – e.g. computer system with computer readable medium having instructions for executing the program), and input and output in HDL [abstract, fig. 2, elements 1-3, fig. 9, element 916].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Chakrabarti and Rostoker because Chakrabarti's method is of a logic synthesis of a digital circuit, and adding Rostoker's HDL, and computer means having instructions for executing the program would have improved Chakrabarti's method by improving design speed and accuracy from using the computer as an automated design tool.

8. Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chakrabarti, et al., "Synthesis of symmetric functions for path-delay fault testability". in view of Minato, "Fast factorization method for implicit cube set representation".

9. As for claims 8-9, Chakrabarti disclosed the invention substantially as claimed, including system for synthesizing a circuit representation having a greater unateness by unate decomposition of SOP and POS circuit representations as cited above in claims 1and 10.

Chakrabarti did not specifically disclose a BDD or zero-suppressed BDD employed to recursively decompose the representation of the sub-circuit into SOP or POS representation.

Minato disclosed a (zero-suppressed) binary decision diagram is employed to recursively decompose the representation of the at least one sub-circuit into the sum-of-products or product-of-sums representation [pg. 377, abstract, sections I. and II.A.; pg. 379, section III.; and pg. 383, section B].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Chakrabarti and Minato because merging Chakrabarti unate expressions would improve Chakrabarti system by allowing for the representation of very large cube sets in an efficient way in order to predict the behavior of such large circuits [See Minato, pg. 377, section I.].

10. Claims 18, 27, and 36-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chakrabarti, et al., "Synthesis of symmetric functions for path-delay fault testability" in view of Rostoker (US Patent 6,470,482), and further in view of Minato, "Fast factorization method for implicit cube set representation".

11. As for claims 18, 27, and 36-37, Chakrabarti disclosed the invention substantially as claimed, including the method of synthesizing a circuit representation including receiving input and output as cited above in the rejections of claims 1-7 (Chakrabarti).

Charkrabarti did not specifically disclose the method performed on a system (means for – e.g. computer system with computer readable medium having instructions for executing the program), and input and output in HDL or using zero-suppressed BDD's.

Chakrabarti in view of Rostoker did not specifically disclose zero-suppressed BDD's.

Rostoker disclosed, a method performed on a system (means for – e.g. computer system with computer readable medium having instructions for executing the program), and input and output in HDL [abstract, fig. 2, elements 1-3, fig. 9, element 916].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Chakrabarti and Rostoker because Chakrabarti's method is of a logic synthesis of a digital circuit, and adding Rostoker's HDL, and computer means having instructions for executing the program would have improved Chakrabarti's method by improving design speed and accuracy from using the computer as an automated design tool.

Minato disclosed a (zero-suppressed) binary decision diagram is employed to recursively decompose the representation of the at least one sub-circuit into the sum-of-products or product-of-sums representation [pg. 377, abstract, sections I. and II.A.; pg. 379, section III.; and pg. 383, section B].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Chakrabarti in view of Rostoker and Minato because employing zero-suppressed BDD's in Chakrabarti in view of Rostoker's unate expressions would improve Chakrabarti in view of Rostoker's system by allowing for the representation of very large cube sets in an efficient way in order to predict the behavior of such large circuits [See Minato, pg. 377, section I.].

12. Applicant's arguments with respect to claims 1-38, have been considered but are moot in view of the new ground(s) of rejection.

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stacy A Whitmore whose telephone number is (703) 305-0565. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (703) 308-3325. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Stacy A Whitmore
Patent Examiner
Art Unit 2812

SAW